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10/065,378	10/10/2002	Sheng-Chung Wu	JCLA6435	1015

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J C PATENTS, INC.
4 VENTURE, SUITE 250
IRVINE, CA 92618

EXAMINER	
TRUONG, BAO Q	
ART UNIT	PAPER NUMBER
2187	3

DATE MAILED: 04/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/065,378	Applicant(s) WU ET AL.	
	Examiner Bao Q Truong	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-8,12 and 13* is/are rejected.

7)☒ Claim(s) *3-5 and 9-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The instant application having Application No. 10/065,378 has a total of 13 claims pending in the application; there are 3 independent claims and 10 dependent claims, all of which are ready for examination by the examiner.

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. § 1.63.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Taiwan on 7 November 2001. It is noted that applicant has filed a certified copy of the Taiwan 90127631 application as required by 35 U.S.C. 119(b).

Drawings

4. The applicant's drawings submitted are acceptable for examination purposes.

Claim Objections

5. Claims 8 and 13 are objected to because of the following informalities:

Claim 8: line 2, "from the first bus in" should be changed to "from the first bus into".

Claim 13: line 6, "anda PCI controller" should be changed to "and a PCI controller".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2, 6-8, and 12-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Young (U.S. Patent No. 5,991,819).

Referring to claim 1, Young teaches a method of operating a control chip having a multiple-layer defer queue between a first bus and a second bus (see figure 3-4), the method comprising:

storing a request in the multiple-layer defer queue, wherein the request is issued by the first bus as receiving requests from a CPU and storing the requests in a Pending Buffer (see figure 4: element 435; and column 9: lines 15-52);

issuing a defer response or a retry response with respect to the request to the first bus as loading the requests into a Pending Buffer to be deferred or retried (see figure 4: elements 417, 435, 437; column 9: lines 42-52; column 16: lines 37-67; and column 17: lines 1-31);

issuing the request to the second bus as sending the requests from the I/O Inbound Request Queue to a PCI device couple to an I/O bus (see figure 3: elements 309A-B; and column 14: lines 47-53);

receiving a responded data with respect to the request from the second bus as receiving data with respect to the requests from the I/O bus at an Outbound Data Buffer (see figure 5E: element 511; and column 14: lines 57-63);

providing the responded data to the first bus if the defer response issues to the first bus as providing data in response to the requests (see figure 5F: element 503; and column 12: lines 62-67); and

providing the responded data to the first bus if the retry response issues to the first bus and only when the first bus again issues the request as in response to the requests that are loaded into the Pending Buffer to be retried, providing data after the requests are retried (see column 17: lines 19-31).

As to claim 2, Young further teaches that, in the step of storing the request into the multiple-layer defer queue, the multiple-layer defer queue also provides a request record with respect to the request as providing an address/command record (see column 9: lines 27-41).

As to claim 6, Young further teaches that the requests includes one selected from the group consisting of at least one input/output (I/O) read request, at least one I/O write request, and at least one memory read request as CPU read/write requests to PCI device (see figures 3 and 4).

Referring to claim 7, Young teaches a method of operating a control chip having a multiple-layer defer queue between a first bus and a second bus (see figures 3-4), the method comprising:

storing a plurality of requests issued from the first bus in the multiple-layer defer queue as receiving requests from a CPU and storing the requests in a Pending Buffer (see figure 4: element 435; and column 9: lines 15-52), wherein each of the requests has corresponding one response selected from the group consisting of a retry response and a defer response to be responded to the first bus as loading the requests into a Pending Buffer to be deferred or retried (see figure 4: elements 417, 435, 437; column 9: lines 42-51; column 16: lines 37-67; and column 17: lines 1-31);

sequentially issuing the requests to the second bus, wherein the requests at least includes a first request as sending the requests from the I/O Inbound Request Queue to a PCI device couple to an I/O bus (see figure 3: elements 309A-B; and column 14: lines 47-53);

receiving a responded data with respect to the first request from the second bus as receiving data with respect to the requests from the I/O bus at an Outbound Data Buffer (see figure 5E: element 511; and column 14: lines 57-63);

providing the responded data to the first bus if the defer response with respect to the first request issues to the first bus as providing data in response to the requests (see figure 5F: element 503; and column 12: lines 62-67); and

providing the responded data to the first bus if the retry response with respect to the first request issues to the first bus and only when the first bus again issues the first request as in

response to the requests that are loaded into the Pending Buffer to be retried, providing data after the requests are retried (see column 17: lines 19-31).

As to claim 8, Young further teaches that, in the step of storing the requests issued from the first bus into the multiple-layer defer queue, the multiple-layer defer queue also provides a request record with respect to the request as providing an address/command record (see column 9: lines 27-41).

As to claim 12, Young further teaches that the requests includes one selected from the group consisting of at least one input/output (I/O) read request, at least one I/O write request, and at least one memory read request as CPU read/write requests to PCI device (see figures 3 and 4).

Referring to claim 13, Young discloses a control chip with multi-layer defer queue (see figures 3-4), coupled to a CPU bus and a PCI bus, the control chip comprising:

a PCI request queue, receiving a CPU request from the CPU bus, and generating a PCI request record (see figure 4: element 405; and column 9: lines 15-40);

a multi-layer defer queue, when receiving the CPU request, respectively responding to the CPU bus by one of a defer response and a retry response as receiving requests from a CPU and storing the requests in a Pending Buffer (see figure 4: element 435; and column 9: lines 15-52); loading the requests into a Pending Buffer to be deferred or retried (see figure 4: elements 417, 435, 437; column 9: lines 42-51; column 16: lines 37-67; and column 17: lines 1-31);

a PCI access queue, receiving the PCI request record (see figure 4: element 417; and column 14: lines 47-53); and

a PCI controller, receiving the request from the multi-layer defer queue, causing the PCI request record of the PCI access queue to be transmitted to the PCI bus via the PO controller (see figure 4: element 413; column 13: lines 40-67; and column 14: lines 1-12);

wherein when the PCI bus generates a response data and if the CPU request in the multi-layer defer queue is to produce the defer response, then the response data is directly sent to CPU bus as providing data in response to the requests (see figure 5F: element 503; and column 12: lines 62-67), if the CPU request in the multi-layer defer queue is to produce the retry response and the CPU bus issues the CPU request, then the response data is transmitted to the CPU bus as in response to the requests that are loaded into the Pending Buffer to be retried, providing data after the requests are retried (see column 17: lines 19-31).

8. Claims 1-2, 6-8, and 12-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Chin et al. (U.S. Patent No. 6,247,102 B1).

Referring to claim 1, Chin teaches a method of operating a control chip having a multiple-layer defer queue between a first bus and a second bus, the method comprising:

storing a request in the multiple-layer defer queue, wherein the request is issued by the first bus as a deferred queue storing CPU-to-PCI transaction cycles (see figure 3: elements 142, 144, 146; column 7: lines 64-67; column 8: lines 1-34);

issuing a defer response or a retry response with respect to the request to the first bus as a deferred queue responding to CPU-to-PCI transaction cycles with either defer response or non-defer (retry) response (see column 30: lines 57-67; and column 31: lines 1-12);

issuing the request to the second bus as sending the CPU-to-PCI transaction cycles to a PCI interface for placing on a PCI device (see figure 2: element 160; and figure 5);

receiving a responded data with respect to the request from the second bus as receiving data with respect to the CPU-to-PCI transaction cycles (see column 22: lines 23-46);

providing the responded data to the first bus if the defer response issues to the first bus; and providing the responded data to the first bus if the retry response issues to the first bus and only when the first bus again issues the request as either deferring a transaction or retrying a transaction cycle (see figures 12; column 22: lines 23-46; column 30: lines 57-67; and column 31: lines 1-12).

As to claim 2, Chin further teaches that, in the step of storing the requests into the multiple-layer defer queue, the multiple-layer defer queue also provides a request record with respect to the request as an in-order queue having a pointer to keep track of transaction cycles (see figure 3: elements 133, 138; column 7: lines 26-28, lines 43-47; and column 8: lines 3-5).

As to claim 6, Chin further teaches that the request includes one selected from the group consisting of an input/output (I/O) read request, an I/O write request, and a memory read request as CPU-to-PCI read/write transactions (see figures 11 and 12).

Referring to claim 7, Chin teaches a method of operating a control chip having a multiple-layer defer queue between a first bus and a second bus, the method comprising:

storing a plurality of requests issued from the first bus in the multiple-layer defer queue as a deferred queue storing CPU-to-PCI transaction cycles (see figure 3: elements 142, 144, 146; column 7: lines 64-67; column 8: lines 1-34), wherein each of the requests has corresponding one response selected from the group consisting of a retry response and a defer response to be responded to the first bus as a deferred queue responding to CPU-to-PCI transaction cycles with either defer response or non-defer (retry) response (see column 30: lines 57-67; and column 31: lines 1-12);

sequentially issuing the requests to the second bus, wherein the requests at least includes a first request as sending the CPU-to-PCI transaction cycles to a PCI interface for placing on a PCI device (see figure 2: element 160; and figure 5);

receiving a responded data with respect to the first request from the second bus as receiving data with respect to the CPU-to-PCI transaction cycles (see column 22: lines 23-46);

providing the responded data to the first bus if the defer response with respect to the first request issues to the first bus and providing the responded data to the first bus if the retry response with respect to the first request issues to the first bus and only when the first bus again issues the first request as either deferring a transaction or retrying a transaction cycle (see figures 12; column 22: lines 23-46; column 30: lines 57-67; and column 31: lines 1-12).

As to claim 8, Chin further teaches that, in the step of storing the requests issued from the first bus into the multiple-layer defer queue, the multiple-layer defer queue also provides a request record with respect to the request as an in-order queue having a pointer to keep track of transaction cycles (see figure 3: elements 133, 138; column 7: lines 26-28, lines 43-47; and column 8: lines 3-5).

As to claim 12, Chin further teaches that the requests includes one selected from the group consisting of at least one input/output (I/O) read request, at least one I/O write request, and at least one memory read request as CPU-to-PCI read/write transactions (see figures 11 and 12).

Referring to claim 13, Chin discloses a control chip with multi-layer defer queue, coupled to a CPU bus and a PCI bus, the control chip comprising:

a PCI request queue, receiving a CPU request from the CPU bus, and generating a PCI request record as a PCI request queue storing CPU to PCI transactions (see figure 3: element 134; and column 7: lines 36-63);

a multi-layer defer queue, when receiving the CPU request, respectively responding to the CPU bus by one of a defer response and a retry response as a deferred queue responding to CPU transactions with either defer response or non-defer (retry) response (see figure 3: elements 142, 144, 146; column 7: lines 64-67; column 8: lines 1-34; column 30: lines 57-67; and column 31: lines 1-12);

a PCI access queue, receiving the PCI request record as a CPU to PCI queue (see figure 2: element 184); and

a PCI controller, receiving the request from the multi-layer defer queue, causing the PCI request record of the PCI access queue to be transmitted to the PCI bus via the PO controller as a PCI interface (see figure 2: element 16; and figure 5);

wherein when the PCI bus generates a response data and if the CPU request in the multi-layer defer queue is to produce the defer response, then the response data is directly sent to CPU bus, if the CPU request in the multi-layer defer queue is to produce the retry response and the CPU bus issues the CPU request, then the response data is transmitted to the CPU bus as either deferring a transaction or retrying a transaction (see figures 12; column 22: lines 23-46; column 30: lines 57-67; and column 31: lines 1-12).

Allowable Subject Matter

9. Claims 3-5 and 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form PTO-892.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bao Q Truong whose telephone number is (703) 308-7090. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

BAO QUOC TRUONG
BT
Patent Examiner
19 April 2004

Donald Sparks
Supervisory Patent Examiner
Technology Center 2100